WHAT IS CLAIMED IS:

1. A structure of a non-volatile flash memory that is a NOR type non-volatile flash memory, which provides floating gates and a common source line, wherein:

a region overlapped one of drains and one of said floating gates in a memory cell is larger than a region overlapped a source and one of said floating gates in said memory cell.

2. A structure of a non-volatile flash memory that is a NOR type non-volatile flash memory, which provides floating gates and a common source line, wherein:

the difference (a−b) between a region " a "overlapped one of drains and one of said floating gates in a memory cell, and a region " b "overlapped a source and one of said floating gates in said memory cell is 0.02 μ m or more.

3. A structure of a non-volatile flash memory that is a NOR type non-volatile flash memory, which provides floating gates and a common source line, wherein:

the impurity gradient distribution of a source in a memory cell at the adjacent position, where said source joints a semiconductor substrate, is formed to be gradual.

4. A structure of a non-volatile flash memory that is a NOR type non-volatile flash memory, which provides floating gates and a common source line in accordance with claim 1, wherein:

said source is composed of first sources and a second source, and said first source and said second source are formed in a state that said first and second sources are contacted with one another, and said first sources are formed at regions overlapped with said floating gates.

5. A structure of a non-volatile flash memory that is a NOR type non-volatile flash memory, which provides floating gates and a common source line in accordance with claim 2, wherein:

said source is composed of first sources and a second source, and said first sources and said second source are formed in a state that said first and second sources are contacted with one another, and said first sources are formed at regions overlapped with said floating gates.

6. A structure of a non-volatile flash memory that is a NOR type non-volatile flash memory, which provides floating gates and a common source line in accordance with claim 4, wherein:

the impurity concentration of said second source is higher than that of said first sources.

7. A structure of a non-volatile flash memory that is a NOR type non-volatile flash memory, which provides floating gates and a common source line in accordance with claim 5, wherein:

the impurity concentration of said second source is higher than that of said first sources.

8. A structure of a non-volatile flash memory that is a NOR type non-volatile flash memory, which provides floating gates and a common source line in accordance with claim 4, wherein:

said source composed of said first and second sources is formed in a state that said first and second sources are unified.

9. A structure of a non-volatile flash memory that is a NOR type non-volatile flash memory, which provides floating gates and a common source line in accordance with claim 5, wherein:

said source composed of said first and second sources is formed

in a state that said first and second sources are unified.

10. A structure of a non-volatile flash memory that provides plural memory cells isolated by isolation regions, comprising:

plural floating gates;

plural drains; and

one source, wherein:

said one source is a common source for said plural memory cells, and impurity concentration of said one source is lower than that of said plural drains.

11. A structure of a non-volatile flash memory that provides plural memory cells isolated by isolation regions in accordance with claim 10, wherein:

said plural memory cells are composed as a pair.

12. A structure of a non-volatile flash memory that provides plural memory cells isolated by isolation regions in accordance with claim 10, wherein:

the number of said plural floating gates and the number of said plural drains are the same.

13. A manufacturing method of a non-volatile flash memory that provides plural memory cells which are isolated by isolation regions, and each of said plural memory cells provides a floating gate, a drain, and one source, wherein:

heat treatment after diffused impurity to said one source is suppressed compared with heat treatment after diffused impurity to said drains.

14. A manufacturing method of a non-volatile flash memory that provides plural memory cells which are isolated by isolation regions, and each of said plural memory cells provides a floating gate, a drain, and one source, wherein:

impurity concentration of said one source is lower than that of said plural drains.

15. A manufacturing method of a non-volatile flash memory that provides plural memory cells which are isolated by isolation regions, and each of said plural memory cells provides a floating gate, a drain, and one source, wherein:

the impurity gradient distribution of said one source in said plural memory cells at the adjacent position, where said one source joints a semiconductor substrate, is formed to be gradual.